Rev. 1.0, Oct. 2014

MZHPV128HDGM-00000
MZHPV256HDGL-00000
MZHPV512HDGL-00000

M.2 PCIe Gen3 SSD

(NAND based Solid State Drive)

datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
0.5	Preliminary version	Aug. 14, 2014	Preliminary	Lucia Kim
1.0	Final version	Oct. 15, 2014	Final	Lucia Kim

SM951 Series

PART NUMBER	MZHPV128HDGM-00000	MZHPV256HDGL-00000	MZHPV512HDGL-00000
Capacity[1]	128GB	256GB	512GB
LBA[2]	250,069,680	500,118,192	1,000,215,216

FEATURES

- PCIe Gen3 8Gb/s Interface, up to 4 Lanes
- Compliant with PCI Express Base Specification Rev. 3.0
- Support Standard AHCI driver
- Power Saving Modes:
  - Supporting APM
  - Supporting L1.2 Mode
- Support NCQ (Up to 32 depth) Command Set
- Support SSD Enhanced S.M.A.R.T. Feature Set
- Support TRIM Command
- End-to-End Data Protection
- RoHS Compliant

Drive Configuration

Capacity	128/256/512GB
From Factor	M.2
Interface	PCIe Gen3 8Gb/s x4
Bytes per Sector	512 Bytes

Performance Specifications

Data Transfer Rate (128KB)	
Sequential Read	(512GB) Up to 2150 MB/s
	(256GB) Up to 2150 MB/s
	(128GB) Up to 2000 MB/s
Sequential Write	(512GB) Up to 1500 MB/s
	(256GB) Up to 1200 MB/s
	(128GB) Up to 600 MB/s
Data I/O Speed (4KB)	
Random Read	(512GB) Up to 90K IOPS
	(256GB) Up to 90K IOPS
	(128GB) Up to 90K IOPS
Random Write	(512GB) Up to 70K IOPS
	(256GB) Up to 70K IOPS
	(128GB) Up to 70K IOPS

Reliability Specifications

UBER	< 1 sector per 10^{15} bits read
MTBF	1.5 Million Hours

Environmental Specifications

Temperature	
Operating	0°C to 70°C
Non-operating	-40°C to 85°C
Humidity (non-condensing)	
Non-operating	5 ~ 95 %
Linear Shock (1/2 sine pulse, 0.5ms)	
Non-operating	1,500 G
Vibration (sine swept, 10~2000Hz, 15min/axis, 3axis)	
Non-operating	
10 ~ 2000 Hz	20 G

Electrical Specifications

Supply Voltage	+3.3V ± 5%
Voltage Ripple/Noise (max.)	100mV p-p
Active (typical)	6.5W
Idle (typical)	50mW
L1.2 (Typ)	2mW

Physical Dimension

Width	22.00 ± 0.15 mm
Length	80.00 ± 0.15 mm
Height	
(Double Side)	Max. 3.73 mm
(Sigle Side)	Max. 2.38 mm
Weight	Up to 10 g

Specifications are subject to change without notice.

1) 1MB = 1,000,000 Bytes, 1GB = 1,000,000,000 Bytes, Unformatted Capacity. User accessible capacity may vary depending on operating environment and formatting.

2) 1 Sector = 512Bytes, Max. LBA represents the total user addressable sectors in LBA mode and calculated by IDEMA rule

3) Actual performance may vary depending on use conditions and environment.

Table Of Contents

1.0 INTRODUCTION

1.1 General Description

This document describes the specification of SM951 SSD which uses PCIe interface.

The SM951 is fully consist of semiconductor device and using NAND Flash Memory which has a high reliability and a high technology in a small form factor for using a SSD and supporting PCIe interface up to 4 lanes shows much faster performance than previous SATA SSDs.
The SM951 provides 128GB, 256GB and 512GB capacity. It's sequential performance is up to 2150MB/s for read operation and 1500MB/s for write operation by 4 lanes. It's random performance is up to 90k IOPS for read and 70k IOPS for write operation by 4 lanes. It could also provide rugged features with an extreme environment with a high MTBF.

1.2 Product List

[Table 1] Product Line-up

Type	Capacity	Part Number
M.2	128GB	MZHPV128HDGM-00000
	256GB	MZHPV256HDGL-00000
	512GB	MZHPV512HDGL-00000

1.3 Ordering Information

M	Z	X	X	X	X	X	X	X	X	X	X	X	-	X	X	X	X	X
1	2	3	4	5	6	7	8	9	10	11	12	13	-	14	15	16	17	18

1. Memory (M)

2. Module Classification
Z: SSD

3. Form Factor
H: PCIe SATAe Ultra-thin

4. Line-Up
P: PM PC/Client

5. SSD CTRL
V: BX

6~8. SSD Density
128: 128GB
256: 256GB
512: 512GB

9. NAND PKG + NAND Voltage
H: BGA (LF,HF)

10. Flash Generation
D: 5th Generation

11~12. NAND Density
GM: 512G ODP 8CE
GL: 1TB HDP 16CE

13. "-"

14. Default
"0"

15. HW revision
0: No revision

16. Packaging type
0: Bulk

17~18. Customer
00: General

2.0 PRODUCT SPECIFICATION

2.1 Capacity

[Table 2] User Addressable Sectors

Capacity	Max LBA
128GB[1)]	250,069,680
256GB[1)]	500,118,192
512GB[1)]	1,000,215,216

NOTE:
1) Gigabyte(GB) = 1,000,000,000 Bytes, 1 Sector = 512Bytes

2.2 Performance[1)]

[Table 3] Drive Performance

Parameter	Unit	NCQ	128GB	256GB	512GB
Sequential Read[1)] (Up to)	MB/s	QD = 32	2,000	2,150	2,150
Sequential Write[2)] (Up to)	MB/s	QD = 32	600	1,200	1,500
Random Read[3)] (Up to)	IOPS	QD = 32	90K	90K	90K
Random Write[3)] (Up to)	IOPS	QD = 32	70K	70K	70K

NOTE:
1) Performance measured using IOMeter 2008 on Windows 8 64bit. Actual performance may vary depending on use conditions and environment
2) Sequential performance measured using 128KB data size.
3) Random performance measured using 4KB data size.

2.3 Power

[Table 4] Maximum Ratings

Parameter		Specifications
Supply Voltage	Allowable voltage	3.3V ± 5%
	Allowable noise/ripple	100mV p-p or less

[Table 5] Power Consumption for M.2 (3.3V Supply)

Parameter		Specifications
Power Consumption	Active (Typical)	6.5 W
	Idle (Typical)	50 mW

2.4 Reliability

This chapter provides the information for the reliability features of the SSD.

2.4.1 MTBF

MTBF is Mean Time Between Failure, and is the predicted elapsed time between inherent failures of a system during operation. As same word, AFR(annual failure ratio) is 0.4%. MTBF can be calculated as the arithmetic average time between failures of a system.

[Table 6] MTBF Specifications

Capacity	MTBF
128GB	1,500,000 Hours
256GB	
512GB	

2.4.2 UBER

UBER is Uncorrectable Bit Error Rate.

[Table 7] UBER Specifications

Parameter	Specification
UBER	< 1 sector per 10^{15} bits read

2.5 Environmental Specification

[Table 8] Temperature, Humidity, Shock, Vibration

Parameter	Mode	Specification
Temperature[1)]	Operating	0°C to 70°C
	Non-operating	-40°C to 85°C
Humidity[2)]	Non-operating	5% to 95%
Shock[3)]	Non-operating	1500G
Vibration[4)]	Non-operating	20G

NOTE:
1) Temperature specification is following JEDEC standard; Expressed temperature must be measured right on the case
2) Humidity is measured in non-condensing
3) Test condition for shock: 0.5ms duration with half sine wave
4) Test condition for vibration: 10Hz to 2000Hz, 15mins/axis on 3axis

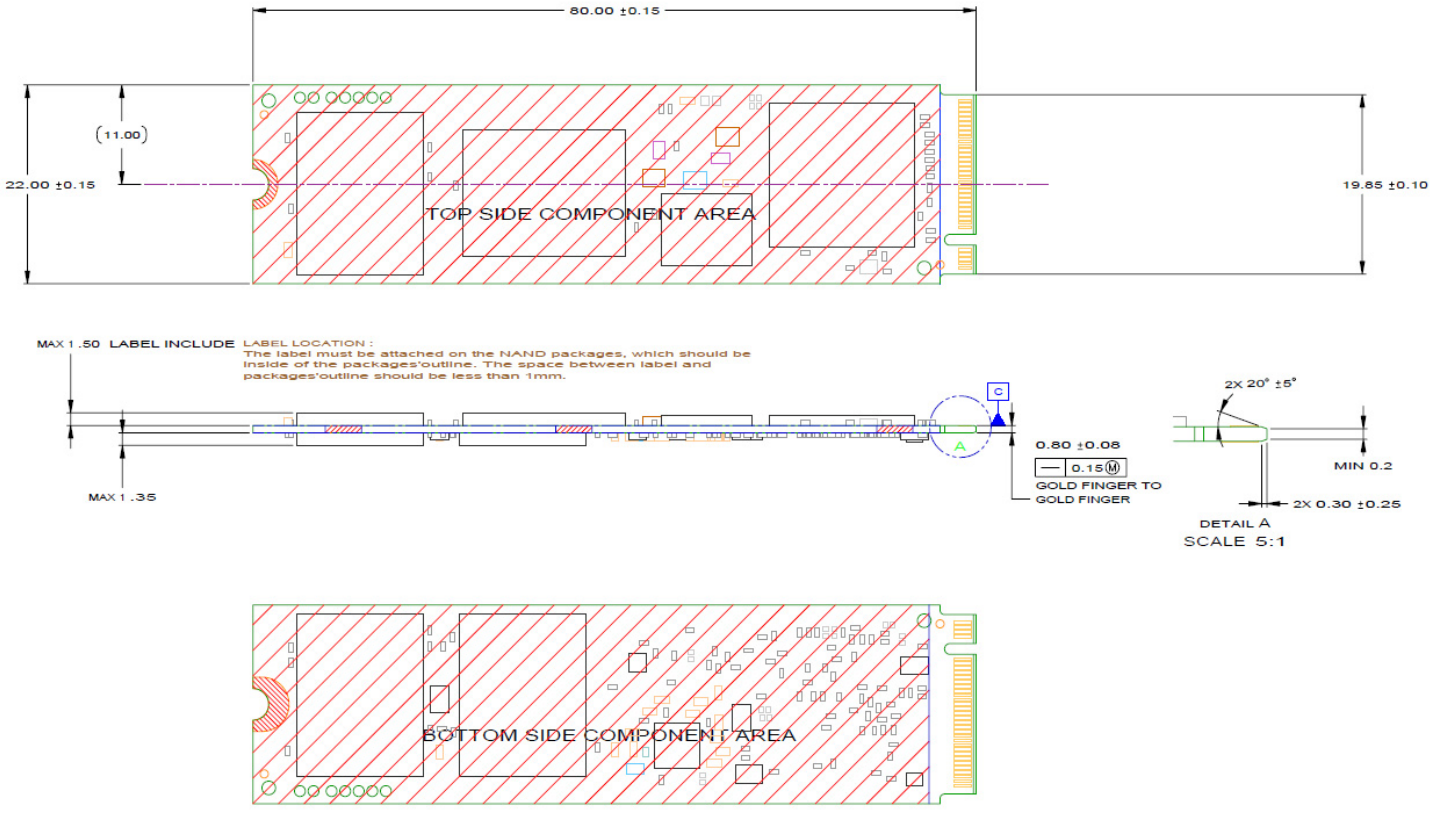
3.0 MECHANICAL SPECIFICATION

3.1 Physical dimensions and Weight

[Table 9] Physical dimensions and Weight

Parameter		Value
Width		22.00 ± 0.15 mm
Length		80.00 ± 0.15 mm
Thickness		3.73 mm
Weight	128/256GB	Max 8g
	512GB	Max 9.5g

3.2 Form Factor

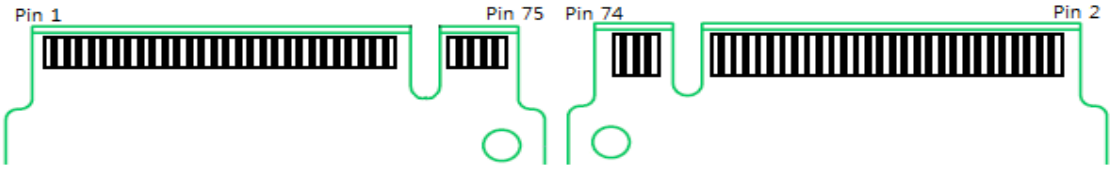


[Figure 1] M.2 Package

4.0 INTERFACE SPECIFACION

4.1 Connector Dimension and Pin Location

[TOP VIEW] [BOTTOM VIEW]



[Figure 2] M.2 Signal and Power pins

4.2 Pin Assignments and Definition

[Table 10] Signal Assignments

Pin#	Assignment	Description	Pin#	Assignment	Description
1	GND	Return current path	2	3.3V	3.3V source
3	GND	Return current path	4	3.3V	3.3V source
5	PETn3	PCIe TX	6	N/C	N/C
7	PETp3	PCIe TX	8	N/C	N/C
9	GND	Return current path	10	LED1#	Device Active Signal
11	PERn3	PCIe Rx	12	3.3V	3.3V source
13	PERp3	PCIe Rx	14	3.3V	3.3V source
15	GND	Return current path	16	3.3V	3.3V source
17	PETn2	PCIe TX	18	3.3V	3.3V source
19	PETp2	PCIe TX	20	N/C	N/C
21	GND	Return current path	22	N/C	N/C
23	PERn2	PCIe Rx	24	N/C	N/C
25	PERp2	PCIe Rx	26	N/C	N/C
27	GND	Return current path	28	N/C	N/C
29	PETn1	PCIe TX	30	N/C	N/C
31	PETp1	PCIe TX	32	N/C	N/C
33	GND	Return current path	34	N/C	N/C
35	PERn1	PCIe Rx	36	N/C	N/C
37	PERp1	PCIe Rx	38	N/C	N/C
39	GND	Return current path	40	N/C	N/C
41	PETn0	PCIe TX	42	N/C	N/C
43	PETp0	PCIe TX	44	N/C	N/C
45	GND	Return current path	46	N/C	N/C
47	PERn0	PCIe Rx	48	N/C	N/C
49	PERp0	PCIe Rx	50	PERST#	PCIe Reset
51	GND	Return current path	52	CLKREQ#	PCIe Device Clock Request
53	REFCLKN	PCIe Reference Clock	54	N/C	N/C
55	REFCLKP	PCIe Reference Clock	56	N/C	N/C
57	GND	Return current path	58	N/C	N/C
67	N/C	N/C	68	N/C	N/C
69	N/C	N/C	70	3.3V	3.3V source
71	GND	Return current path	72	3.3V	3.3V source
73	GND	Return current path	74	3.3V	3.3V source
75	GND	Return current path			

5.0 Command Descriptions

5.1 Supported ATA Commands

[Table 11] Supported ATA Command set

Command Name	Command Code (Hex)	Command Name	Command Code (Hex)
DATA SET MANAGEMENT	06h	WRITE MULTIPLE	C5h
READ SECTOR(S)	20h	SET MULTIPLE MODE	C6h
READ SECTOR(S) EXT	24h	READ DMA	C8h
READ DMA EXT	25h	WRITE DMA	CAh
READ NATIVE MAX ADDRESS EXT	27h	WRITE MULTIPLE FUA EXT	CEh
READ MULTIPLE EXT	29h	STANDBY IMMEDIATE	E0h
READ LOG EXT	2Fh	IDLE IMMEDIATE	E1h
WRITE SECTOR(S)	30h	STANDBY	E2h
WRITE SECTOR(S) EXT	34h	IDLE	E3h
WRITE DMA EXT	35h	READ BUFFER	E4h
SET MAX ADDRESS EXT	37h	CHECK POWER MODE	E5h
WRITE MULTIPLE EXT	39h	SLEEP	E6h
WRITE DMA FUA EXT	3Dh	FLUSH CACHE	E7h
WRITE LOG EXT	3Fh	WRITE BUFFER	E8h
READ VERIFY SECTOR(S)	40h	READ BUFFER DMA	E9h
READ VERIFY SECTOR(S) EXT	42h	FLUSH CACHE EXT	EAh
WRITE UNCORRECTABLE EXT	45h	WRITE BUFFER DMA	EBh
READ LOG DMA EXT	47h	IDENTIFY DEVICE	ECh
WRITE LOG DMA EXT	57h	SET FEATURES	EFh
READ FPDMA QUEUED	60h	SECURITY SET PASSWORD	F1h
WRITE FPDMA QUEUED	61h	SECURITY UNLOCK	F2h
EXECUTE DEVICE DIAGNOSTIC	90h	SECURITY ERASE PREPARE	F3h
DOWNLOAD MICROCODE	92h	SECURITY ERASE UNIT	F4h
DOWNLOAD MICROCODE DMA	93h	SECURITY FREEZE LOCK	F5h
SMART	B0h	SECURITY DISABLE PASSWORD	F6h
Device Configuration Overlay	B1h	READ NATIVE MAX ADDRESS	F8h
READ MULTIPLE	C4h	SET MAX ADDRESS	F9h

5.2 SECURITY FEATURE Set

The Security mode features allow the host to implement a security password system to prevent unauthorized access to the disk drive.

5.2.1 SECURITY mode default setting

The master password is not set and the lock function disabled.
The system manufacturer/dealer may set a new master password by using the SECURITY SET PASSWORD command, without enabling the lock function.

5.2.2 Initial setting of the user password

When a user password is set, the drive automatically enters lock mode by the next powered-on

5.2.3 SECURITY mode operation from power-on

In locked mode, the NSSD rejects media access commands until a SECURITY UNLOCK command is successfully completed.

5.2.4 Password lost

If the user password is lost and High level security is set, the drive does not allow the user to access any data.
However, the drive can be unlocked using the master password.

If the user password is lost and Maxim security level is set, it is impossible to access data.
However, the drive can be unlocked using the ERASE UNIT command with the master password. The drive will erase all user data and unlock the drive.

5.3 SMART FEATURE Set (B0h)

The SMART Feature Set command provides access to the Attribute Values, the Attribute Thresholds, and other low level subcommands that can be used for logging and reporting purposes and to accommodate special user needs. The SMART Feature Set command has several separate subcommands which are selectable via the device's Features Register when the SMART Feature Set command is issued by the host. In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the SMART Feature Set command.

5.3.1 Sub Command

In order to select a subcommand the host must write the subcommand code to the device's Features Register before issuing the S.M.A.R.T. Function Set command. The subcommands and their respective codes are listed below.

[Table 12] S.M.A.R.T. Sub Command set

Subcommand	Code	Subcommand	Code
SMART READ DATA	D0h	SMART WRITE LOG	D6h
SMART READ ATTRIBUTE THRESHOLDS	D1h	SMART ENABLE OPERATIONS	D8h
SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE	D2h	SMART DISABLE OPERATIONS	D9h
SMART SAVE ATTRIBUTE VALUES	D3h	SMART RETURN STATUS	DAh
SMART EXECUTE OFF-LINE IMMIDIATE	D4h	SMART ENABLE/ DISABLE AUTOMATIC OFF-LINE	DBh
SMART READ LOG	D5h		

5.3.1.1 S.M.A.R.T. Read Attribute Values (subcommand D0h)

This subcommand returns the device's Attribute Values to the host. Upon receipt of the S.M.A.R.T. Read Attribute Values subcommand from the host, the device asserts BSY, saves any updated Attribute Values to the Attribute Data sectors, asserts DRQ, clears BSY, asserts INTRQ, and then waits for the host to transfer the 512 bytes of Attribute Value information from the device via the Data Register.

5.3.1.2 S.M.A.R.T. Read Attribute Thresholds (subcommand D1h)

This subcommand returns the device's Attribute Thresholds to the host. Upon receipt of the S.M.A.R.T. Read Attribute Thresholds subcommand from the host, the device reads the Attribute Thresholds from the Attribute Threshold sectors and then waits for the host to transfer the 512 bytes of Attribute Thresholds information from the device.

5.3.1.3 S.M.A.R.T. Enable/Disable Attribute Autosave (subcommand D2h)

This subcommand enables and disables the attribute auto save feature of the device. The S.M.A.R.T. Enable/Disable Attribute Autosave subcommand allows the device to automatically save its updated Attribute Values to the Attribute Data Sector at the timing of the first transition to Active idle mode and after 10 minutes after the last saving of Attribute Values. This subcommand causes the auto save feature to be disabled. The state of the Attribute Autosave feature—either enabled or disabled—will be preserved by the device across the power cycle.
A value of 00h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand—will cause this feature to be disabled. Disabling this feature does not preclude the device from saving Attribute Values to the Attribute Data sectors during some other normal operation such as during a power-up or a power-down.
A value of F1h—written by the host into the device's Sector Count Register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand—will cause this feature to be enabled. Any other nonzero value written by the host into this register before issuing the S.M.A.R.T. Enable/Disable Attribute Autosave subcommand will not change the current Autosave status. The device will respond with the error code specified in Table 7-9: “S.M.A.R.T. Error Codes” on page 30.
The S.M.A.R.T. Disable Operations subcommand disables the auto save feature along with the device's S.M.A.R.T. operations.
Upon the receipt of the subcommand from the host, the device asserts BSY, enables or disables the Autosave feature, clears BSY, and asserts INTRQ.

5.3.1.4 S.M.A.R.T. Save Attribute Values (subcommand D3h)

This subcommand causes the device to immediately save any updated Attribute Values to the device's Attribute Data sector regardless of the state of the Attribute Autosave feature. Upon receipt of the S.M.A.R.T. Save Attribute Values subcommand from the host, the device asserts BSY, writes any updated Attribute Values to the Attribute Data sector, clears BSY, and asserts INTRQ.

5.3.1.5 S.M.A.R.T. Execute Off-line Immediate (subcommand D4h)

This subcommand causes the device to immediately initiate the set of activities that collect Attribute data in an off-line mode (off-line routine) or execute a self-test routine in either captive or off-line mode. The LBA Low register shall be set to specify the operation to be executed.

[Table 13] Execute S.M.A.R.T Sub Command set

LBA Low	Subcommand
00h	Execute S.M.A.R.T. off-line data collection routine immediately
01h	Execute S.M.A.R.T. Short self-test routine immediately in off-line mode
02h	Execute S.M.A.R.T. Extended self-test routine immediately in off-line mode
03h	Reserved
04h	Execute S.M.A.R.T. Selective self-test routine immediately in off-line mode
40h	Reserved
7Fh	Abort off-line mode self-test routine
81h	Execute S.M.A.R.T. short self-test routine immediately in captive mode
82h	Execute S.M.A.R.T. Extended self-test routine immediately in captive mode
84h	Execute S.M.A.R.T. selective self-test routine immediately in captive mode
C0h	Reserved

Off-line mode: The device executes command completion before executing the specified routine. During execution of the routine the device will not set BSY nor clear DRDY. If the device is in the process of performing its routine and is interrupted by a new command from the host, the device will abort or suspend its routine and service the host within two seconds after receipt of the new command. After servicing the interrupting command, the device will resume its routine automatically or not start its routine depending on the interrupting command.

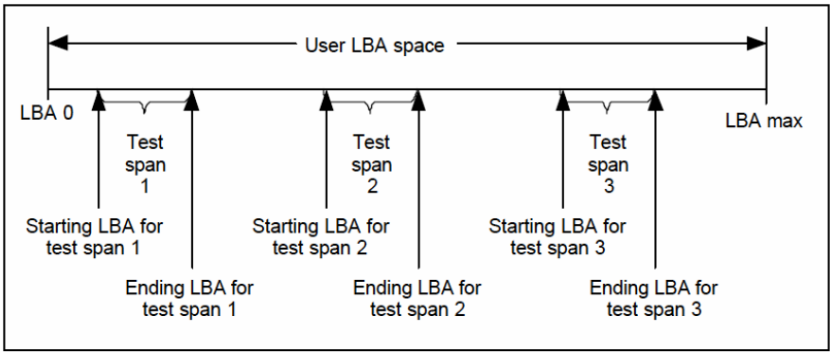
Captive mode: When executing self-test in captive mode, the device sets BSY to one and executes the specified self-test routine after receipt of the command. At the end of the routine, the device sets the execution result in the Self-test execution status byte (see Table 7-1: “Device Attribute Data Structure” on page 23) and ATA registers and then executes the command completion. See definitions below.

Status	Set ERR to one when the self-test has failed
Error	Set ABRT to one when the self-test has failed
LBA Low	Set to F4h when the self-test has failed
LBA High	Set to 2Ch when the self-test has failed

5.3.1.6 S.M.A.R.T. Selective self-test routine

When the value in the LBA Low register is 4 or 132, the Selective self-test routine shall be performed. This self-test routine shall include the initial tests performed by the Extended self-test routine plus a selectable read scan. The host shall not write the Selective self-test log while the execution of a Selective self-test command is in progress.

The user may choose to do read scan only on specific areas of the media. To do this, user shall set the test spans desired in the Selective self-test log and set the flags in the Feature flags field of the Selective self-test log to indicate do not perform off-line scan. In this case, the test spans defined shall be read scanned in their entirety. The Selective self-test log is updated as the self-test proceeds indicating test progress. When all specified test spans have been completed, the test is terminated and the appropriate self-test execution status is reported in the SMART READ DATA response depending on the occurrence of errors. Figure 3 shows an example of a Selective self-test definition with three test spans defined. In this example, the test terminates when all three test spans have been scanned.



[Figure 3] S.M.A.R.T self-test example

After the scan of the selected spans described above, a user may wish to have the rest of media read scanned as an off-line scan. In this case, the user shall set the flag to enable off-line scan in addition to the other settings. If an error occurs during the scanning of the test spans, the error is reported in the self-test execution status in the SMART READ DATA response and the off-line scan is not executed. When the test spans defined have been scanned, the device shall then set the off-line scan pending and active flags in the Selective self-test log to one, the span under test to a value greater than five, the self-test execution status in the SMART READ DATA response to 00h, set a value of 03h in the off-line data collection status in the SMART READ DATA response and shall proceed to do an off-line read scan through all areas not included in the test spans. This off-line read scan shall completed as rapidly as possible, no pauses between block reads, and any errors encountered shall not be reported to the host. Instead error locations may be logged for future reallocation. If the device is powered-down before the off-line scan is completed, the off-line scan shall resume when the device is again powered up. From power-up, the resumption of the scan shall be delayed the time indicated in the Selective self-test pending time field in the Selective self-test log. During this delay time the pending flag shall be set to one and the active flag shall be set to zero in the Selective self-test log. Once the time expires, the active flag shall be set to one, and the off-line scan shall resume. When the entire media has been scanned, the off-line scan shall terminate, both the pending and active flags shall be cleared to zero, and the off-line data collection status in the SMART READ DATA response shall be set to 02h indicating completion.

During execution of the Selective self-test, the self-test executions time byte in the Device SMART Data Structure may be updated but the accuracy may not be exact because of the nature of the test span segments. For this reason, the time to complete off-line testing and the self-test polling times are not valid. Progress through the test spans is indicated in the selective self-test log.

A hardware or software reset shall abort the Selective self-test except when the pending bit is set to one in the Selective self-test log (see 7.3.7). The receipt of a SMART EXECUTE OFF-LINE IMMEDIATE command with 0Fh, Abort off-line test routine, in the LBA Low register shall abort Selective self-test regardless of where the device is in the execution of the command. If a second self-test is issued while a selective self-test is in progress, the selective self-test is aborted and the newly requested self-test is executed.

5.3.1.7 S.M.A.R.T. Read Log Sector (subcommand D5h)

This command returns the indicated log sector contents to the host. Sector count specifies the number of sectors to be read from the specified log. The log transferred by the drive shall start at the first sector in the specified log, regardless of the sector count requested. Sector number indicates the log sector to be returned as described in the following Table.

[Table 14] Log Sector

Log sector address	Content	
00h	Log directory	RO
01h	SMART error log	RO
02h	Comprehensive SMART error log	RO
04h-05h	Reserved	RO
06h	SMART self-test log	RO
08h	Reserved	RO
09h	Selective self-test log	RW
0Ah-7Fh	Reserved	RO
80h-9Fh	Host vendor specific	R/W
A0h-FFh	Reserved	VS

RO - Log is read only by the host.
R/W - Log is read or written by the host.
VS - Log is vendor specific thus read/write ability is vendor specific.

5.3.1.8 S.M.A.R.T. Write Log Sector (subcommand D6h)

This command writes 512 bytes of data to the specified log sector. The 512 bytes of data are transferred at a command and the LBA Low value shall be set to one. The LBA Low shall be set to specify the log sector address. If a Read Only log sector is specified, the device returns ABRT error.

5.3.1.9 S.M.A.R.T. Enable Operations (subcommand D8h)

This subcommand enables access to all S.M.A.R.T. capabilities within the device. Prior to receipt of a S.M.A.R.T. Enable Operations subcommand, Attribute Values are neither monitored nor saved by the device. The state of S.M.A.R.T.—either enabled or disabled—will be preserved by the device across power cycles. Once enabled, the receipt of subsequent S.M.A.R.T. Enable Operations subcommands will not affect any of the Attribute Values. Upon receipt of the S.M.A.R.T. Enable Operations subcommand from the host, the device asserts BSY, enables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

5.3.1.10 S.M.A.R.T. Disable Operations (subcommand D9h)

This subcommand disables all S.M.A.R.T. capabilities within the device including the device's attribute auto save feature. After receipt of this subcommand the device disables all S.M.A.R.T. operations. Non self-preserved Attribute Values will no longer be monitored. The state of S.M.A.R.T.—either enabled or disabled—is preserved by the device across power cycles. Note that this subcommand does not preclude the device's power mode attribute auto saving.

Upon receipt of the S.M.A.R.T. Disable Operations subcommand from the host, the device asserts BSY, disables S.M.A.R.T. capabilities and functions, clears BSY, and asserts INTRQ.

After receipt of the device of the S.M.A.R.T. Disable Operations subcommand from the host, all other S.M.A.R.T. subcommands—with the exception of S.M.A.R.T. Enable Operations—are disabled, and invalid and will be aborted by the device—including the S.M.A.R.T. Disable Operations subcommand—returning the error code as specified in Table 7-9: “S.M.A.R.T. Error Codes” on page 30.

Any Attribute Values accumulated and saved to volatile memory prior to receipt of the S.M.A.R.T. Disable Operations command will be preserved in the device's Attribute Data Sectors. If the device is re-enabled, these Attribute Values will be updated, as needed, upon receipt of a S.M.A.R.T. Read Attribute Values or a S.M.A.R.T. Save Attribute Values command.

5.3.1.11 S.M.A.R.T. Return Status (subcommand DAh)

This subcommand is used to communicate the reliability status of the device to the host's request. Upon receipt of the S.M.A.R.T. Return Status subcommand the device asserts BSY, saves any updated Attribute Values to the reserved sector, and compares the updated Attribute Values to the Attribute Thresholds.

If the device does not detect a Threshold Exceeded Condition, or detects a Threshold Exceeded Condition but involving attributes are advisory, the device loads 4Fh into the LBA Mid register, C2h into the LBA High register, clears BSY, and asserts INTRQ.

If the device detects a Threshold Exceeded Condition for pre-failure attributes, the device loads F4h into the LBA Mid register, 2Ch into the LBA High register, clears BSY, and asserts INTRQ. Advisory attributes never result in a negative reliability condition.

5.3.1.12 S.M.A.R.T. Enable/Disable Automatic Off-line (subcommand DBh)

This subcommand enables and disables the optional feature that cause the device to perform the set of off-line data collection activities that automatically collect attribute data in an off-line mode and then save this data to the device's nonvolatile memory. This subcommand may either cause the device to automatically initiate or resume performance of its off-line data collection activities or cause the automatic off-line data collection feature to be disabled. This subcommand also enables and disables the off-line read scanning feature that cause the device to perform the entire read scanning with defect reallocation as the part of the off-line data collection activities.

The Sector Count register shall be set to specify the feature to be enabled or disabled:

Sector Count	Feature Description
00h	Disable Automatic Off-line
F8h	Enable Automatic Off-line

A value of zero written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic off-line data collection feature to be disabled. Disabling this feature does not preclude the device from saving attribute values to nonvolatile memory during some other normal operation such as during a power-on, during a power-off sequence, or during an error recovery sequence.

A value of F8h written by the host into the device's Sector Count register before issuing this subcommand shall cause the automatic Off-line data collection feature to be enabled.

Any other non-zero value written by the host into this register before issuing this subcommand is vendor specific and will not change the current Automatic Off-Line Data Collection and Off-line Read Scanning status. However, the device may respond with the error code specified in Table 26: “S.M.A.R.T. Error Codes”.

5.3.2 Device Attribute Data Structure

The following defines the 512 bytes that make up the Attribute Value information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Values subcommand.

[Table 15] Device Attribute Data Structure

Byte	Descriptions
0~1	Data structure revision number
2~361	1st - 30th Individual attribute data
362	Off-line data collection status
363	Self-test execution status
364~365	Total time in seconds to complete off-line data collection activity
366	Vendor Specific
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability 7-1 Reserved 0 1=Device error logging supported
371	Self-test failure check point
372	Short self-test routine recommended polling time(in minutes)
373	Extended self-test routine recommended polling time(in minutes)
374-510	Reserved
511	Data structure checksum

5.3.2.1 Data Structure Revision Number

The Data Structure Revision Number identifies which version of this data structure is implemented by the device.
This revision number will be set to 0001h. This revision number identifies both the Attribute Value and Attribute Threshold Data structures.

5.3.2.2 Individual Attribute Data Structure

The following defines the 12 bytes that make up the information for each Attribute entry in the Device Attribute Data Structure.

[Table 16] Attribute Data Structure

Byte	Descriptions
0	Attribute ID number 01-FFh
1~2	Status flag bit 0 (pre-failure/advisory bit) bit 0 = 0: If attribute value is less than the threshold, the drive is in advisory condition. Product life period may expired. bit 0 = 1: If attribute value is less than the threshold, the drive is in pre-failure condition. The drive may have failure. bit 1 (on-line data collection bit) bit 1 = 0: Attribute value will be changed during off-line data collection operation. bit 1 = 1: Attribute value will be changed during normal operation. bit 2 (Performance Attribute bit) bit 3 (Error rate Attribute bit) bit 4 (Event Count Attribute bit) bit 5 (Self-Preserving Attribute bit) bit 6-15 Reserved
3	Attribute value 01h-FDh *1 00h, FEh, FFh = Not in use 01h = Minimum value 64h = Initial value FDh = Maximum value
4	Worst Ever normalized Attribute Value (valid values from 01h-FEh)
5~10	Raw Attribute Value Attribute specific raw data (FFFFFFh - reserved as saturated value)
11	Reserved (00h)
*1 For ID = 199 CRC Error Count	

Attribute ID Numbers:
Any nonzero value in the Attribute ID Number indicates an active attribute. The device supports following Attribute ID Numbers.

ID	Attribute Name	ID	Attribute Name	ID	Attribute Name
05h	Reallocated Sector Count	ADh	Average Program / Erase Count	C2h	Temperature
09h	Power-on Hours Count	AEh	Unexpected Power Loss Count	C7h	SATA CRC Error Count
0Ch	Power Cycle Count	B2h	Used Reserved Block Count	E9h	NAND GB Written
AAh	Grown Bad Blocks	B4h	Unused Reserved Block Count	F1h	Host GB Written
ABh	Program Fails	B8h	End to End Data Errors Corrected	F2h	Host GB Read
ACh	Erase Fails	BBh	Uncorrectable Error Count		

5.3.2.3 Off-Line Data Collection Status

The value of this byte defines the current status of the off-line activities of the device. Bit 7 indicates an Automatic Off-line Data Collection Status.
Bit 7 Automatic Off-line Data Collection Status
0 Automatic Off-line Data Collection is disabled.
1 Automatic Off-line Data Collection is enabled.

Bits 0–6 represent a hexadecimal status value reported by the device.

Value	Definition
0	Off-line data collection never started.
2	All segments completed without errors. In this case the current segment pointer is equal to the total segments required.
3	Off-line activity in progress.
4	Off-line data collection is suspended by the interrupting command.
5	Off-line data collecting is aborted by the interrupting command.
6	Off-line data collection is aborted with a fatal error.

5.3.2.4 Self-test execution status

Bit	Definition
0-3	Percent Self-test remaining. An approximation of the percent of the self-test routine remaining until completion given in ten percent increments. Valid values are 0 through 9.
4-7	Current Self-test execution status.
	0 The self-test routine completed without error or has never been run.
	1 The self-test routine was aborted by the host.
	2 The self-test routine was interrupted by the host with a hard or soft reset.
	3 The device was unable to complete the self-test routine due to a fatal error or unknown test error.
	4 The self-test routine was completed with an unknown element failure.
	5 The self-test routine was completed with an electrical element failure.
	6 The self-test routine was completed with a servo element failure.
	7 The self-test routine was completed with a read element failure.
	15 The self-test routine is in progress.

5.3.2.5 Total time in seconds to complete off-line data collection activity

This field tells the host how many seconds the device requires to complete the off-line data collection activity.

5.3.2.6 Current segment pointer

This byte is a counter indicating the next segment to execute as an off-line data collection activity. Because the number of segments is 1, 01h is always returned in this field.

5.3.2.7 Off-line data collection capability

Bit	Definition
0	Execute Off-line Immediate implemented bit
	0 S.M.A.R.T. Execute Off-line Immediate subcommand is not implemented
	1 S.M.A.R.T. Execute Off-line Immediate subcommand is implemented
1	Enable/disable Automatic Off-line implemented bit
	0 S.M.A.R.T. Enable/disable Automatic Off-line subcommand is not implemented
	1 S.M.A.R.T. Enable/disable Automatic Off-line subcommand is implemented
2	Abort/restart off-line by host bit
	0 The device will suspend off-line data collection activity after an interrupting command and resume it after a vendor specific event
	1 The device will abort off-line data collection activity upon receipt of a new command Bit Definition
3	Off-line Read Scanning implemented bit
	0 The device does not support Off-line Read Scanning
	1 The device supports Off-line Read Scanning
4	Self-test implemented bit
	0 Self-test routing is not implemented
	1 Self-test routine is implemented
5	Reserved (0)
6	Selective self-test routine is not implemented
	0 Selective self-test routine is not implemented
	1 Selective self-test routine is implemented
7	Reserved (0)

5.3.2.8 S.M.A.R.T. Capability

This word of bit flags describes the S.M.A.R.T. capabilities of the device. The device will return 03h indicating that the device will save its Attribute Values prior to going into a power saving mode and supports the S.M.A.R.T. ENABLE/DISABLE ATTRIBUTE AUTOSAVE command.

Bit	Definition
0	Pre-power mode attribute saving capability. If bit = 1, the device will save its Attribute Values prior to going into a power saving mode (Standby or Sleep mode).
1	Attribute auto save capability. If bit = 1, the device supports the S.M.A.R.T. ENABLE/ DISABLE ATTRIBUTE AUTOSAVE command.
2-15	Reserved (0)

5.3.2.9 Error logging capability

Bit	Definition
7-1	Reserved (0)
0	The Error Logging support bit. If bit = 1, the device supports the Error Logging

5.3.2.10 Self-test failure check point

This byte indicates the section of self-test where the device detected a failure.

5.3.2.11 Self-test completion time

These bytes are the minimum time in minutes to complete the self-test.

5.3.2.12 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

5.3.3 Device Attribute Thresholds data structure

The following defines the 512 bytes that make up the Attribute Threshold information. This data structure is accessed by the host in its entirety using the S.M.A.R.T. Read Attribute Thresholds. All multi-byte fields shown in these data structures follow the ATA/ATAPI-6 specification for byte ordering, that is, that the least significant byte occupies the lowest numbered byte address location in the field.
The sequence of active Attribute Thresholds will appear in the same order as their corresponding Attribute Values.

[Table 17] Attribute Thresholds Data Structure

Byte	Descriptions
0~1	Data structure revision number
2~361	1st - 30th Individual attribute data
362 ~ 379	Reserved
380 ~ 510	Vendor specific
511	Data structure checksum

5.3.3.1 Data Structure Revision Number

This value is the same as the value used in the Device Attributes Values Data Structure.

5.3.3.2 Individual Thresholds Data Structure

The following defines the 12 bytes that make up the information for each Threshold entry in the Device Attribute Thresholds Data Structure. Attribute entries in the Individual Threshold Data Structure are in the same order and correspond to the entries in the Individual Attribute Data Structure.

[Table 18] Threshold Data Structure

Byte	Descriptions
0	Attribute ID Number (01h to FFh)
1	Attribute Threshold (for comparison with Attribute Values from 00h to FFh) 00h - “always passing” threshold value to be used for code test purposes 01h - minimum value for normal operation FDh - maximum value for normal operation FEh - invalid for threshold value FFh - “always failing” threshold value to be used for code test purposes
2~11	Reserved (00h)

5.3.3.3 Attribute ID Numbers

Attribute ID Numbers supported by the device are the same as Attribute Values Data Structures.

5.3.3.4 Attribute Threshold

These values are preset at the factory and are not meant to be changeable. However, the host might use the “S.M.A.R.T. Write Attribute Threshold” sub-command to override these preset values in the Threshold sectors.

5.3.3.5 Data Structure Checksum

The Data Structure Checksum is the 2's compliment of the result of a simple 8-bit addition of the first 511 bytes in the data structure.

5.3.4 S.M.A.R.T. Log Directory

The following defines the 512 bytes that make up the S.M.A.R.T. Log Directory. The S.M.A.R.T. Log Directory is on S.M.A.R.T. Log Address zero and is defined as one sector long.

[Table 19] S.M.A.R.T. Log Directory

Byte	Descriptions
0~1	S.M.A.R.T. Logging Version
2	Number of sectors in the log at log address 1
3	Reserved
4	Number of sectors in the log at log address 2
5	Reserved
...	
510	Number of sectors in the log at log address 255
511	Reserved

The value of the S.M.A.R.T. Logging Version word shall be 01h. The logs at log addresses 80-9Fh are defined as 16 sectors long.

5.3.5 S.M.A.R.T. error log sector

The following defines the 512 bytes that make up the S.M.A.R.T. error log sector. All multi-byte fields shown in these data structures follow the ATA/ATAPI-6 specifications for byte ordering.

[Table 20] S.M.A.R.T. Error Log Sector

Byte	Descriptions
0	S.M.A.R.T. error log version
1	Error log pointer
2-91	1st error log data structure
92-181	2nd error log data structure
182-271	3rd error log data structure
272-361	4th error log data structure
362-451	5th error log data structure
452-453	Device error count
454-510	Reserved
511	Data structure checksum

5.3.5.1 S.M.A.R.T. error log version

This value is set to 01h.

5.3.5.2 Error log pointer

This points to the most recent error log data structure. Only values 1 through 5 are valid.

5.3.5.3 Device error count

This field contains the total number of errors. The value will not roll over.

5.3.5.4 Error log data structure

The data format of each error log structure is shown below.

[Table 21] Error Data Structure

Byte	Descriptions
n ~ n+11	1st command data structure
n+12 ~ n+23	2nd command data structure
n+24 ~ n+35	3rd command data structure
n+36 ~ n+47	4th command data structure
n+48 ~ n+59	5th command data structure
n+60 ~ n+89	Error data structure

5.3.5.5 Command data structure

Data format of each command data structure is shown below.

[Table 22] Command Data Structure

Byte	Descriptions
n	Content of the Device Control register when the Command register was written
n+1	Content of the Features Control register when the Command register was written
n+2	Content of the Sector Count Control register when the Command register was written
n+3	Content of the LBA Low register when the Command register was written
n+4	Content of the LBA Mid register when the Command register was written
n+5	Content of the LBA High register when the Command register was written
n+6	Content of the Device/Head register when the Command register was written
n+7	Content written to the Command register
n+8	Timestamp
n+9	Timestamp
n+10	Timestamp
n+11	Timestamp

Timestamp shall be the time since power-on in milliseconds when command acceptance occurred. This timestamp may wrap around.

5.3.5.6 Error data structure

Data format of error data structure is shown below.

[Table 23] Error Data Structure

Byte	Descriptions
n	Reserved
n+1	Content written to the Error register after command completion occurred.
n+2	Content written to the Sector Count register after command completion occurred.
n+3	Content written to the LBA Low register after command completion occurred.
n+4	Content written to the LBA Mid register after command completion occurred.
n+5	Content written to the LBA High register after command completion occurred.
n+6	Content written to the Device/Head register after command completion occurred.
n+7	Content written to the Status register after command completion occurred.
n+8 - n+26	Extended error information
n+27	State
n+28	Life Timestamp (least significant byte)
n+29	Life Timestamp (most significant byte)

Extended error information will be vendor specific.

State field contains a value indicating the device state when command was issued to the device.

Value	State
x0h	Unknown
x1h	Sleep
x2h	Standby
x3h	Active/Idle with BSY cleared to zero
x4h	Executing SMART off-line or self-test
x5h-xAh	Reserved
xBh-xFh	Vendor unique

The value of x is vendor specific and may be different for each state.

5.3.6 Self-test log structure

The following defines the 512 bytes that make up the Self-test log sector.

[Table 24] Self-test Log Structure

Byte	Byte
0~1	Data structure revision
n*24+2	Self-test number
n*24+3	Self-test execution status
n*24+4~n*24+5	Life timestamp
n*24+6	Self-test failure check point
n*24+7~n*24+10	LBA of first failure
n*24+11~n*24+25	Vendor specific
...	...
506~507	Vendor specific
508	Self-test log pointer
509~510	Reserved
511	Data structure checksum

NOTE:
N is 0 through 20

The data structure contains the descriptor of the Self-test that the device has performed. Each descriptor is 24 bytes long and the self-test data structure is capable to contain up to 21 descriptors. After 21 descriptors has been recorded, the oldest descriptor will be overwritten with the new descriptor. The self-test log pointer points to the most recent descriptor. When there is no descriptor, the value is 0. When there are descriptor(s), the value is 1 through 21.

5.3.7 Selective self-test log data structure

The Selective self-test log is a log that may be both written and read by the host. This log allows the host to select the parameters for the self-test and to monitor the progress of the self-test. The following table defines the contents of the Selective self-test log which is 512 bytes long. All multi-byte fields shown in these data structures follow the specifications for byte ordering.

[Table 25] Self-test Log Data Structure

Byte	Description	Read/Write
0-1	Data structure revision	R/W
2-9	Starting LBA for test span 1	R/W
10-17	Ending LBA for test span 1	R/W
18-25	Starting LBA for test span 2	R/W
26-33	Ending LBA for test span 2	R/W
34-41	Starting LBA for test span 3	R/W
42-49	Ending LBA for test span 3	R/W
50-57	Starting LBA for test span 4	R/W
58-65	Ending LBA for test span 4+	R/W
66-73	Starting LBA for test span 5	R/W
74-81	Ending LBA for test span 5	R/W
82-337	Reserved	Reserved
338-491	Vendor specific	Vendor specific
492-499	Current LBA under test	Read
500-501	Current span under test	Read
502-503	Feature flags	R/W
504-507	Vendor Specific	Vendor specific
508-509	Selective self test pending time	R/W
510	Reserved	Reserved
511	Data structure checksum	R/W

5.3.8 Error reporting

The following table shows the values returned in the Status and Error Registers when specific error conditions are encountered by a device.

[Table 26] S.M.A.R.T. Error Codes

Error condition	Status Register	Error Register
A S.M.A.R.T. FUNCTION SET command was received by the device without the required key being loaded into the LBA High and LBA Mid registers.	51h	04h
A S.M.A.R.T. FUNCTION SET command was received by the device with a subcommand value in the Features Register that is either invalid or not supported by this device.	51h	04h
A S.M.A.R.T. FUNCTION SET command subcommand other than S.M.A.R.T. ENABLE OPERATIONS was received by the device while the device was in a “S.M.A.R.T. Disabled” state.	51h	04h
The device is unable to read its Attribute Values or Attribute Thresholds data structure	51h	10h or 04h
The device is unable to write to its Attribute Values data structure.	51h	10h or 40h

6.0 PRODUCT COMPLIANCE

6.1 Product regulatory compliance and Certifications

[Table 27] Certifications and Declarations

Category	Certification
CE	Comunaute Europeenne
BSMI	Bureau of Standards, Metrology and Inspection
KCC	Korea Communications commission
VCCI	Voluntary Control Council for Interference
C-Tick	Radio Telecommunication Labeling
FCC	Federal Communications Commission
IC	Industry Canada
UL	Underwriters Laboratories, Inc.
TUV	Technischer Uberwachungs Verine .e.V
CB	Scheme of the IECEE for Mutual Recognition of Test Certificates for Electrical Equipment

Caution: Any changes or modifications in construction of this device which are not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications, However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Modifications not expressly approved by the manufacturer could void the user's authority to operated the equipment under FCC rules.

1. 기자재 명칭 : SSD (Solid State Drive)
2. 모델명(Model): 라벨 별도 표기
3. 제조연월 : 라벨 별도 표기
4. 제조자 : 삼성전자(주)
5. 제조국가 : 대한민국
6. 상호명 : 삼성전자(주)

Industry Canada ICES-003 Compliance Label:
CAN ICES-3 (B)/NMB-3(B)

7.0 Identify Device Data

[Table 28] Returned values

Word	128GB	256GB	512GB	Description
0	0040h	0040h	0040h	General information
1	3FFFh	3FFFh	3FFFh	Obsolete
2	C837h	C837h	C837h	Specific configuration
3	0010h	0010h	0010h	Obsolete
4-5	0000h	0000h	0000h	Retired
6	003Fh	003Fh	003Fh	Obsolete
7-8	0000h	0000h	0000h	Reserved for the CompactFlash Association
9	0000h	0000h	0000h	Retired
10-19	XXXXh	XXXXh	XXXXh	Serial Number (ATA string)
20-21	0000h	0000h	0000h	Retired
22	0000h	0000h	0000h	Obsolete
23-26	XXXXh	XXXXh	XXXXh	Firmware revision (ATA string)
27-46	XXXXh	XXXXh	XXXXh	Model number (ATA string)
47	8010h	8010h	8010h	Number of sectors on multiple commands
48	4000h	4000h	4000h	Trusted Computing feature set options
49	2F00h	2F00h	2F00h	Capabilities
50	4000h	4000h	4000h	Capabilities
51-52	0200h	0200h	0200h	Obsolete
53	0007h	0007h	0007h	Words Validity
54	3FFFh	3FFFh	3FFFh	Obsolete
55	0010h	0010h	0010h	Obsolete
56	003Fh	003Fh	003Fh	Obsolete
57	FC10h	FC10h	FC10h	Obsolete
58	00FBh	00FBh	00FBh	Obsolete
59	0110h	0110h	0110h	Multiple sector setting
60	C2B0h	FFFFh	FFFFh	Total number of user addressable logical sectors for 28-bit commands
61	0EE7h	0FFFh	0FFFh	Total number of user addressable logical sectors for 28-bit commands
62	0000h	0000h	0000h	Obsolete
63	0007h	0007h	0007h	Multi-word DMA transfer
64	0003h	0003h	0003h	Flow control PIO transfer modes supported
65	0078h	0078h	0078h	Minimum Multi-word DMA transfer cycle time per word
66	0078h	0078h	0078h	Manufacturer's recommended Multi-word DMA transfer cycle time
67	0078h	0078h	0078h	Minimum PIO transfer cycle time without flow control
68	0078h	0078h	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	0F00h	0F00h	0F00h	Additional supported
70-74	0000h	0000h	0000h	Reserved
75	001Fh	001Fh	001Fh	Queue depth
76	850Eh	850Eh	850Eh	Serial ATA capabilities
77	0006h	0006h	0006h	Reserved for future Serial ATA definition
78	0064h	0064h	0064h	Serial ATA features supported
79	0060h	0060h	0060h	Serial ATA features enabled
80	03FCh	03FCh	03FCh	Major version number
81	0039h	0039h	0039h	Minor version number
82	346Bh	346Bh	346Bh	Commands and feature sets supported
83	7D09h	7D09h	7D09h	Commands and feature sets supported
84	4163h	4163h	4163h	Commands and feature sets supported
85	3469h	3469h	3469h	Commands and feature sets supported or enabled
86	BC09h	BC09h	BC09h	Commands and feature sets supported or enabled
87	4163h	4163h	4163h	Commands and feature sets supported or enabled
88	407Fh	407Fh	407Fh	Ultra DMA transfer

89	0003h	0003h	0003h	Time required for Normal Erase mode SECURITY ERASE UNIT command
90	0010h	0010h	0010h	Time required for an Enhanced Erase mode SECURITY ERASE UNIT command
91	0000h	0000h	0000h	Current advanced power management value
92	FFFEh	FFFEh	FFFEh	Master Password Revision Code
93	0000h	0000h	0000h	Hardware reset result
94	0000h	0000h	0000h	Current automatic acoustic management value
95	0000h	0000h	0000h	Stream Minimum Request Size
96	0000h	0000h	0000h	Streaming Transfer Time - DMA
97	0000h	0000h	0000h	Streaming Access Latency - DMA and PIO
98-99	0000h	0000h	0000h	Streaming Performance Granularity (DWord)
100	C2B0h	32B0h	12B0h	Total Number of User Addressable Logical Sectors for 48-bit commands (QWord)
101	0EE7h	1DCFh	3B9Eh	Total Number of User Addressable Logical Sectors for 48-bit commands (QWord)
102-103	0000h	0000h	0000h	Total Number of User Addressable Logical Sectors for 48-bit commands (QWord)
104	0000h	0000h	0000h	Streaming Transfer Time - PIO
105	0008h	0008h	0008h	Maximum number of 512-byte data blocks of LBA Range Entries per DATA SET MANAGEMENT command
106	4000h	4000h	4000h	Physical sector size / logical sector size
107	0000h	0000h	0000h	Inter-seek delay for ISO 7779 standard acoustic testing
108	5002h	5002h	5002h	World wide name
109	5389h	5389h	5389h	World wide name
110-111	XXXXh	XXXXh	XXXXh	World wide name
112-116	0000h	0000h	0000h	Reserved
117-118	0000h	0000h	0000h	Logical sector size (Dword)
119	401Eh	401Eh	401Eh	Commands and feature sets supported
120	401Ch	401Ch	401Ch	Commands and feature sets supported or enabled
121-126	0000h	0000h	0000h	Reserved for expanded supported and enabled settings
127	0000h	0000h	0000h	Obsolete
128	002Xh	002Xh	002Xh	Security status
129-157	0000h	0000h	0000h	Vendor specific
158	0000h	0000h	0000h	Vendor specific
159	0000h	0000h	0000h	Vendor specific
160	0000h	0000h	0000h	CFA power mode
161-167	0000h	0000h	0000h	Reserved for the CompactFlash Association
168	0000h	0000h	0000h	Reserved
169	0001h	0001h	0001h	DATA SET MANAGEMENT is supported
170-205	0000h	0000h	0000h	Additional Product Identifier, Current media serial number (ATA string)
206	003Dh	003Dh	003Dh	SCT Command Transport
207-208	0000h	0000h	0000h	Reserved for CE-ATA
209	4000h	4000h	4000h	Alignment of logical blocks within a physical block
210-211	0000h	0000h	0000h	Write-Read-Verify Sector Count Mode 3
212-213	0000h	0000h	0000h	Write-Read-Verify Sector Count Mode 2
214	0000h	0000h	0000h	NV Cache Capabilities
215-216	0000h	0000h	0000h	NV Cache Size in Logical Blocks (DWord)
217	0001h	0001h	0001h	Nominal media rotation rate
218	0000h	0000h	0000h	Reserved
219	0000h	0000h	0000h	NV Cache Options
220-221	0000h	0000h	0000h	Reserved
222	107Fh	107Fh	107Fh	Transport major version number
223	0000h	0000h	0000h	Transport major version number
224-233	0000h	0000h	0000h	Reserved for CE-ATA
234	0000h	0000h	0000h	Minimum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
235	0800h	0800h	0800h	Maximum number of 512-byte data blocks per DOWNLOAD MICROCODE command for mode 03h
236-254	0000h	0000h	0000h	Reserved
255	XXXXh	XXXXh	XXXXh	Integrity word

8.0 References

[Table 29] Standards References

Item	Website
PCI Express Base Specification Revision 3.0	http://www.pcisig.com/specifications/pciexpress/
PCIe M.2 Electromechanical Specification Revision 1.0	http://www.pcisig.com/
Solid-State Drive (SSD) Requirements and Endurance Test Method (JESD219)	http://www.jedec.org/standards-documents/results/jesd219
Solid-State Drive (SSD) Requirements and Endurance Test Method (JESD218)	http://www.jedec.org/standards-documents/docs/jesd218/
ATA/ATAPI Command Set 3 Specification	http://www.t13.org/
S.M.A.R.T.	http://www.t13.org/